Ruoyu Wang

+86 182-6567-6265 | wangry@shanghaitech.edu.cn
https://aliceeva.github.io

EDUCATION

ShanghaiTech University *Sep 2016 - Jun 2020*

Bachelor, Computer Science, School of Information Science and Technology *Shanghai, China*

- Third-year GPA: 3.86/4.0 (rank 10/115).
- Honors: SIST dean scholarship (2016); Outstanding student (2016, 2017, 2018); Outstanding team leader (2018).
- Relevant Coursework: Computer Architecture III (graduate-level)(A+); Software Engineering (A+); Parallel Computing (A); Programing Language and Compiler (A).

University of Chicago *Jul 2017 - Aug 2017*

Summer School Program *Chicago, USA*

- Taken courses Intensive Academic English for Disciplinary Study (NOND 21003) and Visual Language: On Images (ARTV 10100).

Unversity of Padova *Aug 2018 - Sep 2018*

Summer School Program *Padova, Italy*

- Cross-disciplinary summer school program across Informatics, Arts and Fundamental Sciences.

PUBLICATIONS

- Lu Wang, Leilei Wang, **Ruoyu Wang** and Pingqiang Zhou, "Optimizing the Energy Efficiency of Power Supply in Heterogeneous Multicore Chips with Integrated Switched-Capacitor Converters," Submitted to IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).
- Yu Ma, Dingcheng Jia, Huifan Zhang, **Ruoyu Wang** and Pingqiang Zhou, "A Compact Memory Structure based on 2T1R against Single-Event Upset in RRAM Arrays," Proceedings of the IEEE International Conference on ASIC (ASION), October 2019.

RESEARCH EXPERIENCE

Optimization of the Power Efficiency on Heterogeneous Multi-core Chips *May 2019 - Aug 2019*

Computer Aided Design Group , Supervised by Prof. Pingqiang Zhou *ShanghaiTech University*

Energy efficiency is a major concern in heterogeneous multi-core chip, the switching-capacitor converters (SCC) are widely used in multi-core chips. However, there is an optimization opportunity for efficiency improvement by **selecting proper SCC configurations**. Besides, **dynamic** SCCs selection can also make it more efficient. In this project, I have designed the experiment of dynamic on-chip capacitance allocation, then, proposed to lose a model of static allocation by **introducing lose caused by Vdroop** and implemented in the experiment code. Reconstructed experiment code and made it scalable, evaluated 4, 8, 16 cores chips. Finally, the simulation achieved about **20% efficiency improvement** when comparing the static method. This work finally produced the paper "Optimizing the Energy Efficiency of Power Supply in Heterogeneous Multicore Chips with Integrated Switched-Capacitor Converters". In the project, I have learned how to do optimization simulations and practiced academic writing.

Design Automation Conference (DAC) System Design Contest *Nov 2018 - May 2019*

Computer Aided Design Group , Supervised by Prof. Pingqiang Zhou & Prof. Cheng Zhuo *ShanghaiTech University & ZJU*

The contest is aimed to design an object-detection inference system on a specific GPU (TX2). Teamed with Zhejiang University, our group designed a yolov3 based **inference neural network** and deployed it on TX2. I have simplified the inference network architecture, and accelerated the inference from **3fps to 50fps**, then enhanced the network design, using **feature pyramid network** to make the detection of tiny objects **more accurate**. Finally, we achieved **3rd place** in 52 teams from the world's top universities. The 1st place is the team from the University of Illinois at Urbana-Champaign and 2nd place is the team from Tsinghua University. From the project, I learned how to design neural networks and how to optimize them, also, I learned how to use main-stream neural network frameworks.

2T1R Memory Strucutre Against Single-Event Upset in RRAM Arrays *May 2019 - Aug 2019*

Computer Aided Design Group , Supervised by Prof. Pingqiang Zhou *ShanghaiTech University*

- Investigated the 1-transistor-1-RRAM array structure and analyzed the single-event upset (SEU) effect.
- Evaluated the improvement of 1-transistor-2-RRAM design and proposed the novel 2-transistor-1-RRAM array structure to avoid SEU.

- Achieved 400pJ energy-saving and 1ns delay improvement.
- Published the paper "A Compact Memory Structure based on 2T1R against Single-Event Upset in RRAM Arrays".

Large-Scale Marine Data Correlations Analysis *Sep 2019 - Present*

Laboratory of I/O Systems & Data Science , Supervised by Prof. Shu Yin *ShanghaiTech University*

- Analyzed the internal correlations of large-scale high-dimension marine data (in progress).
- Implemented high-efficiency data extraction methods on large-scale data.
- Demonstrated the correlations between different dimensions of the data (in progress).

PROJECT & LEADERSHIP EXPERIENCE

NcTrace: Optimized Trace Data Storage with the netCDF Format *Mar 2019 - Aug 2019*

- Optimized the storage of comma-separated values (CSV) trace data using the netCDF I/O library. Introduced the "dimension packing" storage model which reduces the file size and accelerates users' analysis tasks.
- Tested with Google cluster traces, and achieved 7:1 size reduction with 2 orders of magnitude acceleration on reading.

pREFA: Presentation Tool for Regular Expressions and Finite Automatons *Sep 2018 - Jan 2019*

- Designed a presentation tool for Regular Expressions(RE) and Finite Automatons(FA) as a public Python library with GUI.
- Adopted "Kamada-Kawai" algorithm to perform automatic human-readable FA graph generation.
- The project is open source: https://github.com/hgz12345ssdlh/prefa-master

The 18th China Fault Tolerant Computing Conference AI Acceleration Forum *Aug 2019 - Aug 2019*

- Implemented a demonstration of an object-detection inference network.
- Led other groups to set up their demo and guided them to prepare for the forum.
- Delivered a 10-minute talk about the design of our network.

TEACHING EXPERIENCE

Advanced Distributed System (CS290K , graduate-level) *Jul 2019 - Aug 2019*

Teaching Assistant *ShanghaiTech University*

- Held office hour for graduate students who have taken this course.
- Revised the project assignment and guided them to accomplish the distributed file system project.

Computer Architecture (CS110, undergraduate-level) *Feb 2019 - Jun 2019*

Teaching Assistant *ShanghaiTech University*

- Designed 2 RISC-V assignments, created problems for three exams and held office hour for students.
- Delivered a lecture about cache to 110 sophomores.

HONORS & AWARDS

- Design Automation Conference System Design Contest 3rd Place Group *Jun 2019*
- ShanghaiTech University Industry Practice Outstanding Team Leader *Sep 2018*
- ShanghaiTech University Outstanding Student *2016, 2017, 2018*
- ShanghaiTech University School of Information Science and Technology Dean Scholarship *Sep 2016*

EXTRACURRICULAR ACTIVITIES

Association President *Sep 2016 - Sep 2019*

- Created a calligraphy association at freshman year and acted as president for 3 years.

Volunteer

- Student volunteer for Anual ShanghaiTech Symposium on Information Science and Technology in 2017 and 2018.

SKILLS LIST

- **Programming Languages:** C/C++, Python, Matlab, Rust.
- **Tool:** CUDA, TensorRT, OpenMP, MPI, Spark, CMake, LaTex, Git